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The Biggest Erasable PROM
Yet Puts 16,384 Bits
on a Chip

Robert Greene, George Perlegos, Phillip J. Salsbury, and William L. Morgan
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The biggest erasable PROM yet puts 16,384 bits on a chip

Using just one 5-V supply, the ultraviolet-erasable device is interchangeable with 16-k read-only memories—a boon to designers of microprocessor systems

by Robert Greene, George Perlegos, Phillip J. Salsbury, and William L. Morgan, *Intel Corp., Santa Clara, Calif.*

☐ In just two or three years, from being barely on the edge of visibility, a field-erasable read-only memory has blazed its way to prominence in the system designer's world. Because its contents can be erased with ultraviolet light, its user can program and reprogram it at will—an unaccustomed liberty.

Known as EPROMs (for erasable programmable ROMs), the devices in heavy use today are the 2,048-bit 1702A and the 8,192-bit 2708, both of which have been designed into a wide variety of equipment over the past few years. But the new 16,384-bit model, which is also faster and easier to use than its predecessors, is bound to attract old and new users alike.

The attraction, of course, is the devices' extreme usefulness for prototyping software code in microprocessor-based designs. It typically takes tens of passes through a system before a program's code can be optimized, and each pass requires a new ROM program. But a ROM that can be erased and reprogrammed quickly from standard address signals makes it much easier to optimize a program.

Indeed, individual words can be rewritten in today's UV-erasable PROMs, so that programmers can fine-tune their software well into the development cycle or change a portion of the program to accommodate new system features. Then, once satisfied with the program, the user can switch into production with factory-programmable ROMs that have identical pin assignments and use similar power supplies.

Alternatively, as the availability of erasable PROMs increases, system designers are beginning to use them in place of standard ROMs in the production equipment itself, especially in the early sample stage and also in small-volume designs. It is an all-too-familiar problem, getting small numbers of mask-programmed ROMs from the factory in anything like a reasonable time and at less than an exorbitant per-piece cost. Here the erasable PROM is the perfect answer, for it goes straight into the equipment once its program is fixed.

A good deal in all respects

The new Intel Corp. 2716 16-k device has all this versatility, and then some (see table). It offers twice the memory capacity on a chip only 20% larger than the 8-k version—and the smaller the die, the lower its production costs eventually fall. Its performance is better. Though its maximum access time stays at a short 450 nanoseconds, its active power dissipation per bit has been reduced to 40% of the 8-k device level, so that the chip's total power dissipation is 20% lower for 16,384 bits than
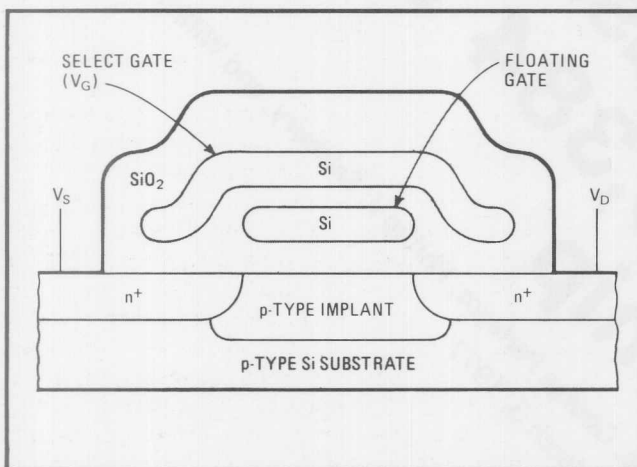
1. Doubling up. By using two levels of polysilicon, this stacked-gate version of the floating-gate avalanche-injection MOS cell occupies half the area of earlier Famos cells. As a result, the 16,384-bit 2716 chip is only 20% larger than the 8,192-bit 2708 devices.
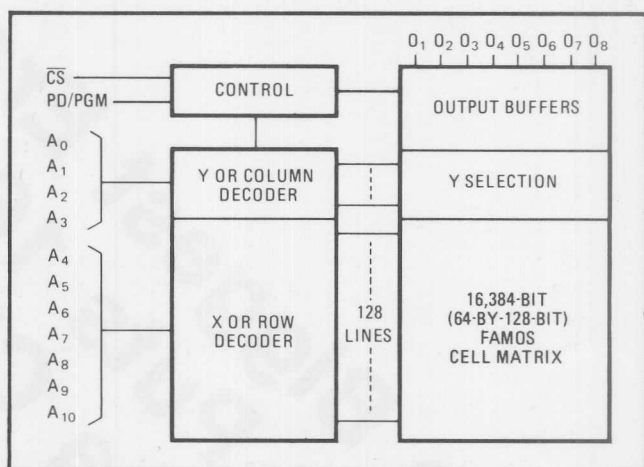
2. Aimed at microcomputers. The 16,384 cells in the 2716 device are organized into two 64-by-128-cell arrays or 2,048 8-bit words, an arrangement that makes the device useful for byte-oriented microcomputer designs and also compatible with 16-k ROMs.

ULTRAVIOLET-LIGHT-ERASABLE PROGRAMMABLE ROMs			
Year	1972	1975	1977
Model	1702A	2708	2716
Basic features			
Technology	p-MOS	n-MOS	n-MOS
Organization	256 X 8	1,024 X 8	2,048 X 8
Chip area (mil^2 equiv.)	134	160	175
Package pins	24	24	24
Read performance			
Access time (max) (ns)	650	450	450
Power dissipation (mW)	700	730	500
'' '' per bit (mW)	0.4	0.1	0.04
Standby power (mW)	*	*	125
'' '' per bit (mW)	*	*	0.006
Power supplies (V)	+5, −9	+5, +12, −5	+5
TTL compatibility	yes	yes	yes
Programming requirements			
Supply voltages (V)	+12, −35, −48	+26, +5, +12, −5	+25, +5
'' '' pulsed, V_P	yes	yes	no
Program control levels (V)	0/−48	0/+12	TTL
Address and data inputs (V)	0/−48	TTL	TTL
Duty cycle (%)	20	80 − 100	80 − 100
Programming performance			
Programming time of all words (s)	120	100	100
'' '' per word (s)	0.4	100	0.05
Single-pulse programming	no	no	yes
Single-location programming	yes	no	yes
Erase time of all words (minutes)	10 − 20	10 − 30	10 − 30

*Power dissipation can be reduced by clocking power supply or turning off during deselect

it was for 8,192 bits. In fact, the 2716's speed-power product, at 450 ns and 500 milliwatts, puts it on a par with standard high-density ROMs. Moreover, the chip's low standby power mode, in which it dissipates only 125 mw, affords further power savings at the system level.

Equally important, the 2716 works off a single 5-volt power supply, in contrast to the earlier multiple-supply 1702A and 2708 devices. This change is vital for today's designs, since it allows the device to be used with the new, more powerful 5-v microcomputers. In fact, another device using the same basic cell concept, the 8755, has been designed with special input/output ports and control lines to work directly with the 5-v Intel 8085 microcomputer, as well as with other types of 5-v microprocessor systems.

In applying the new 16-k 2716 in microprocessor-based systems, the system designer not only replaces two 2708 packages with one 2716, but he or she can also eliminate the 1-of-4 decoder chip that is needed with the two earlier devices. Indeed, when hooking up the 2716 to single-chip microcomputers such as Intel's 8048, only a standard, commercially available 8212 latch is used, as with the 2708 configuration, and nothing else. All other control signals and address signals are supplied by the processor.

Finally, the new devices are easier to program than the earlier ones. They need only two programming supply voltages (+25 and +5 v) instead of three and four different voltage levels (some as high as 48 v) typical of UV-erasable PROMs. Moreover, the program voltage V_P need not be a low-duty-cycle pulse, so that program time is greatly reduced—from 100 seconds to 0.05 s per bit— even while control levels and address and data inputs are

The Famos principle

Famos describes the floating-gate avalanche-injection metal-oxide-semiconductor transistor that Dov Frohman-Bentchkowsky developed at Intel Corp. in 1971.

The Famos device is essentially a silicon-gate MOS field-effect transistor in which no connection is made to the floating silicon gate. Instead, charge is injected into the gate by avalanches of high-energy electrons from either the source or the drain. A voltage of -28 volts applied to the pn junction releases the electrons.

Data is stored in a Famos memory by charging the floating-gate insulator above the channel region. The threshold voltage then changes, and the presence or absence of conduction is the basis for readout.

The Famos cell has generally been considered more reliable than nitride storage mechanism used in reprogrammable metal-nitride-oxide-semiconductor memories. In MNOS memories, carriers tunnel through a thin oxide layer into traps at the oxide-nitride interface. But a partial loss of stored charge during readout limits the number of readout cycles to approximately 10^{11}.

In Famos memories, on the other hand, there is no loss of charge due to reading. Moreover, over time, the loss of stored electrons is negligible, less than one per cell per year. and information retention is excellent.

kept at straight 5-v transistor-transistor-logic levels.

All these improvements flow from a new n-channel stacked-gate cell that uses just one transistor. This cell is fabricated with a dual-layer silicon-gate process that closely resembles the one used in today's 16-k dynamic random-access memories. As the cross section in Fig. 1

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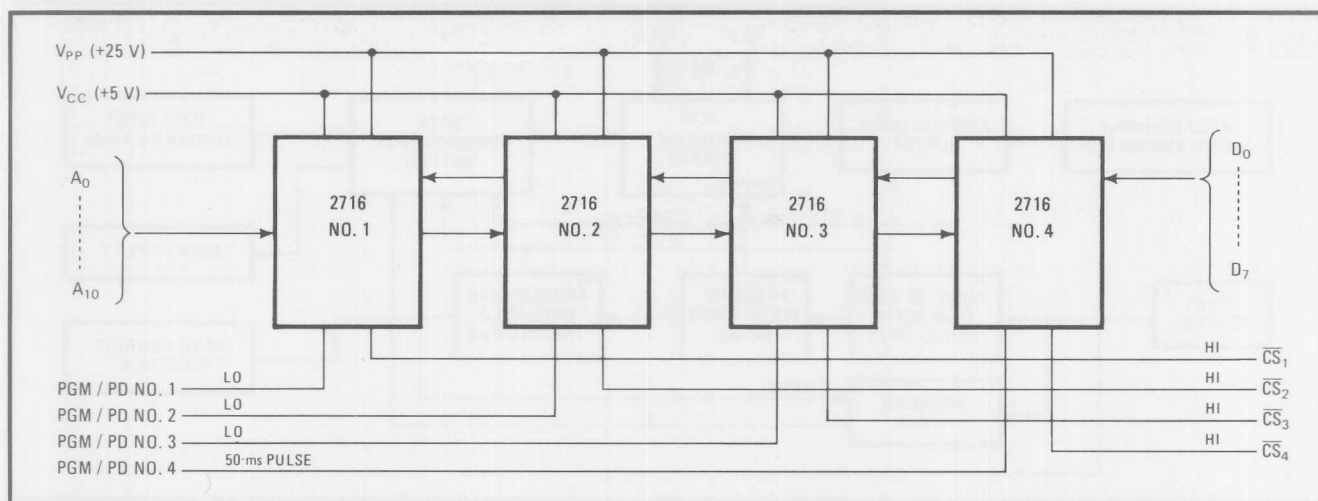
3. Picking and choosing. The 2716 erasable PROM has a program inhibit mode, to allow the designer of a multipackage system to program some of the devices and not others. Only those devices that receive a TTL-level pulse on the PGM/PD pin will be programmed.

shows, a lower floating gate stores the cell's charge, and an upper control or select gate operates the cell. Being stacked one over the other, the gates create an extremely compact structure—the smallest cell of any UV-erasable PROM in production. Including decode, address, drive, and sense circuitry, the entire memory fits on a chip well under 40,000 mil^2 in area.

As for the cell's operation, the fact that it has a fairly complicated stacked-gate configuration is completely transparent to the user. Unlike the 1702A erasable-PROM floating-gate cells (see "The Famos principle," p. 109), the stacked-gate cell is programmed by means of hot electrons injected from the channel through the oxide to the floating gate. This injected charge raises the threshold voltages at the top or select gate, so that a charged cell has a higher select voltage than an uncharged cell. The overall charge pattern, then, as seen from the select gates, duplicates the pattern of a standard mask-ROM.

Once programmed, the charge retention of the new 16-k UV-erasable PROM is as good as in the original Famos devices. Reliability studies of standard production runs indicate that 95% of the devices can be expected to retain their memory for 100 years at 70°C. Charge removal from the stacked-gate cell occurs with its exposure to ultraviolet light, just as in both the earlier UV-erasable devices.

Using the 2716

The array of 16,384 Famos cells, which are formed into two 64-by-128-cell matrixes (Fig. 2), is organized as 2,048 8-bit words, giving the 2716 a byte orientation that is useful in microcomputer applications. Because of this arrangement, the device operates almost exactly like the 2708 8-k erasable-PROM. The only differences are that on the 2708 device the power-supply voltages V_{DD} and V_{BB} are on pin 19 and pin 21 respectively, whereas on the 2716 device the address A_{10} is on pin 19 and the program voltages (+25 v for programming, 5 v for reading) are on pin 21.

Otherwise, complete data and power-supply compatibility exists between the familiar 2708 and the new 2716:

they plug into exactly the same sockets, having exactly the same standard 24-pin package and the same pin assignments (except for those mentioned above). The one change in designing a board with a 2716 is that programming it requires a +25 v power supply and reading it takes a 5-v supply instead of the 26-v pulses needed for programming and the ±12 v, +5 v, and −5 v supplies needed for reading the 2708.

As for ease of use, the 2716 compares well with ordinary ROMs. The seven highest-order address bits, A_4 to A_{10}, select the rows, while address bits A_0 to A_5 select the columns and operate on eight 1-of-16 decoders, such that one of 16 column lines is gated to each of the eight output buffers.

Sensing is the same as in the 2708 devices. The charge on the selected column line is monitored. Unprogrammed cells will have a low threshold and will discharge the column line when selected, while the threshold of programmed cells will have been raised to an impedance level that is high enough to keep the column line charged.

To read the 2716, the chip-select input is the only control input required. Lower this input to a transistor-transistor-logic 0 and the device reads; raise it to a TTL 1 again and the device stops reading—is deselected. When deselected, this chip-select input causes the outputs to go into the high impedance state within about 120 ns, a time short enough to allow a designer to OR-tie several 2716s in parallel yet still retain the maximum 450-ns access times of individual devices. On the other hand, since chip select is really an enabling signal, if only one or two 2716s are being used in a system, they may be left low during all cycles, allowing a designer to exploit the typically faster access times of any individually selected devices.

Writing and erasing are no big chores, either. Initially, and after each erasure, all bits of the 2716 are in the logic 1 state (output high). Data is written by selectively programming 0s (output low) into the desired bit locations. To set up the 2716 for programming, the program power supply, V_{PP}, is raised to 25 v, and the chip-select is raised to the input high-voltage state (V_{IH}) or 2.2 v

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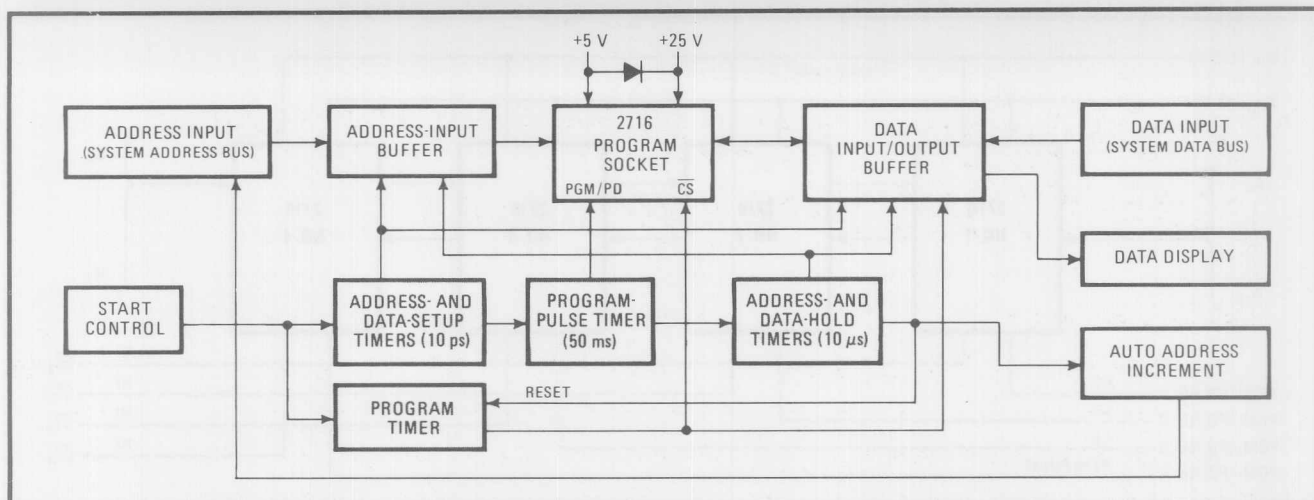
4. Programming made easy. In this setup, the user need only observe the appropriate setup times for the programming operation to succeed. The start control signal gets the timing chain moving, and from then on things are practically automatic.

minimum. The data is then presented, 8 bits in parallel, on the data output lines (O_1 to O_8 in Fig. 2), while the corresponding address is presented to the address inputs.

After the address and data setup times have elapsed, a program pulse is applied to the programming PGM/PD pin. This pulse is a TTL-level signal that serves to gate the program power supply, V_{PP}, into the array. It must be present for at least 50 milliseconds to ensure long-term retention of the programmed data. When this program is completed, the V_{PP} pin should be returned to +5 v.

Finally, erasing the 2716 is the same as for all UV-erasable PROMs. The user places it under an UV lamp and exposes it to the equivalent of 15 watt-seconds/cm². Although there is no evidence that extended exposure harms the device, the lamp should be placed on a timer and shut off after 30 minutes to prevent unduly long (overnight and over-weekend) accidental exposure.

A useful feature of the 2716's program design is its program-inhibit mode. In multipackage systems, this mode lets the designer ignore some of the devices on a given board and only program or reprogram the rest. The setup is shown in Fig. 3. All inputs and outputs are tied together except for PGM/PD. Only those devices that receive a TTL-level pulse on the PGM/PD pin will be programmed. In the setup shown, device No. 4 is being programmed with a 50-millisecond pulse on this pin, while the address contents of the other three devices are unaffected.

The programming schemes devised for the 2716 are easier than for previous UV-erasable PROMs, as may be seen from the example diagrammed in Fig. 4. In this scheme, the addresses and data may be derived from a microcomputer system bus. Alternatively, the user can generate both manually, employing toggle switches for control and a counter for address input. However, when manual operation is performed, a provision must be made for automatic incrementing of the address pulses.

In either case, a start control signal enables the timing chain shown in Fig. 4, assuring that the appropriate setup times are observed. This signal also enables the program timer, which controls the 2716 chip-select

From PROM to final ROM—fast

Since the UV-erasable 16,384-bit 2716 user-programmable ROM is pin-compatible with the 2316E mask-programmed 16-k ROM, designers can debug systems with the 2716 and, as soon as the data pattern is firm, order read-only memories to plug directly into the 2716/2316E socket. In fact, the initial system can be shipped with erasable PROMs and fitted with ROMs in the field when they become available. Also, the 2716 can be used as the master for transmitting the desired data pattern back to the factory without all the hassle of tape formats.

This direct interchangeability between the 2716 and the 2316E can also speed up implementing code changes. In the past, even when systems were successfully prototyped with UV-erasable PROMs and released to production using mask ROMs, the slightest code change forced the end user to wait while the new code was implemented on the prototype system, then translated into a ROM pattern, and only then placed in the production system. But when the 2316E is used in production systems, any change in code can be performed in a matter of a few hours by programming a 2716 with the custom pattern and plugging it in.

signal, and places the data input/output buffer in the input mode. The program timer must be reset after the address and data hold times have passed.

Once started, the address and data-setup timers enable the program pulse timer, which applies the required TTL pulse to the 2716 PGM/PD pin. This pulse, in turn, on its falling edge, enables the address- and data-hold timers. After they have finished, the auto-address-increment timer does one of two things. Either it advances the address-input counter on a manual programmer, or it resets a not-busy flag on a microprocessor. The program timer is then reset, placing the data I/O buffer in the output mode for data verification. Note that the V_{PP} (+25-v) supply does not have to be turned off or switched during program/read transitions. However, it should be lowered to V_{CC} for nonprogramming operation to reduce power dissipation. □